

**AMENDMENTS TO THE DRAWINGS:**

The attached drawing sheet includes amendments to FIGS. 1A-3C. These sheets replace the original sheets including FIGS. 1A-3C. Marked copies of amended FIGS. 1A-3C are also enclosed.

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**REMARKS**

Claims 1, 4, 5 and 9 have been amended to more closely conform to U.S. claiming practice. The abstract and drawing FIGS. 1A-3C have also been amended. No new matter has been entered by any of the foregoing amendments.

Turning to the rejection of claims 1, 2 and 4-6 under 35 USC §102(b) as being anticipated by JP 11-219762 to Sony, independent claims 1, 4, and 5 have each been amended to require, in part, a "circuit board having a plurality of through holes into which a plurality of leads of an electronic device are inserted and soldered with lead-free solder." Sony fails to disclose or suggest lead-free solder utilized in the soldering, as required in the claims. As explained in the Background of the present application (at page 4, lines 7-23), the use of lead-free solder directly relates to the purpose of the present disclosure.

[I]n recent years, due to increasing awareness of environmental issues, environment pollution caused by lead becomes problematic, and a shift to lead-free solder is rapidly promoted. . . . [W]hen lead-free solder is used, the stress generated by difference in thermal expansions and thermal shrinkages between the multi-layer circuit board and the case of the electronic device during the soldering process or the like is increased and the stress reduction effect by solder is decreased, and therefore the stress applied to the circuit board is increased. For that reason, the occurrence rate of the phenomenon in which the circuit board is broken, in particular, at the through hole portion at the outermost end of the electronic device, is increased.

In circuit boards which do not use lead-free solder, as is the case with Sony, the lead-containing, eutectic solder absorbs the stress generated by the differences of thermal expansion between the circuit board and the associated electronic device or the like, thereby reducing the stresses applied to the circuit board. Hence, through hole corner cracks and through hole separations are prevalent in circuit boards which use lead-free solder and are not addressed by Sony.

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Moreover, claims 1, 4, and 5 require a “conductive film is formed on a wall surface of said through holes.” Sony fails to disclose or teach, either explicitly or implicitly, a conductive film formed on a wall surface of said through holes. As the cited art fails to disclose every element of claims 1, 4, and 5, Sony cannot be said to anticipate claims 1, 4, and 5. Further, because Sony is not directed to circuit boards utilizing lead-free solder, Sony cannot be seen to render obvious claims 1, 4, and 5.

Claims 2 and 6 depend from claims 1 and 5 and are allowable over the cited art for at least the reasons claims 1 and 5 are allowable.

The rejection of claim 3 under 35 USC §103 (a) as being unpatentable over Sony is also in error. Claim 3 depends from claim 2, which in turn depends from claim 1. Sony fails to teach every element of claim 1, as articulated above. As claim 3 depends from and, thus, incorporates every requirement of claim 1, Sony fails to teach every requirement of claim 3. As Sony does not teach every requirement of claim 3, Sony cannot be said to render claim 3 obvious.

The rejection of claims 1, 7, and 8 under 35 USC §103 (a) as being unpatentable over JP Laid Open 12375/81 to Mitsumi over Sony is also in error. Claims 7 and 8 depend on independent claim 1. The deficiencies of Sony vis-à-vis claim 1 are discussed above. Similarly, Mitsumi fails to teach lead-free solder utilized in the soldering, as required in the amended claims and, as explained above, directly relates to the purpose of the present disclosure. Further, claim 1 requires a “conductive film is formed on a wall surface of said through holes.” Mitsumi fails to disclose a conductive film is formed on a wall surface of said through holes. Thus, for at least the reasons discussed above, the combination of Sony and Mitsumi cannot render claim 1 obvious.

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Claims 7 and 8 depend from claim 1 and, as Mitsumi in view of Sony fail to disclose every requirement of claim 1, claims 7 and 8 are allowable over the disclosure of Mitsumi in view of Sony.

While not directly addressed in the Office Action, claim 9 is also allowable over the prior art cited. Independent claim 9 includes limitations similar to those distinguishing claims 1-8 from the cited prior art. Thus, a similar rejection of claim 9 would be inappropriate.

Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable action is respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account Number 08-1391.

Respectfully submitted,



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**CERTIFICATE OF ELECTRONIC FILING**

I hereby certify that this paper is being deposited with the United States Patent Office via the electronic filing procedure on September 22, 2009 at Tucson, Arizona.



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Serial No. 10/597,306

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Annotated Marked-up Drawings

Fig. 1A PRIOR ART

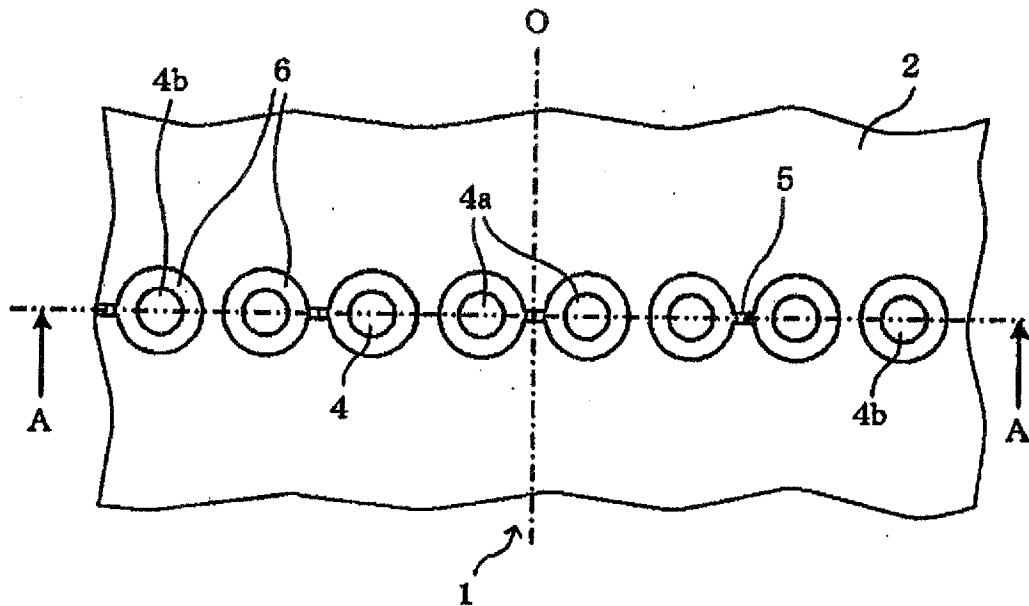


Fig. 1B PRIOR ART

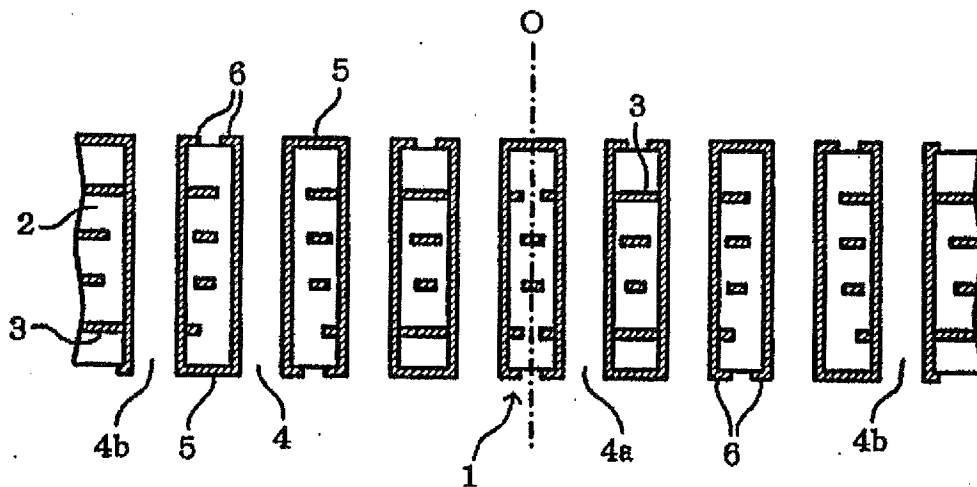


Fig. 2 PRIOR ART

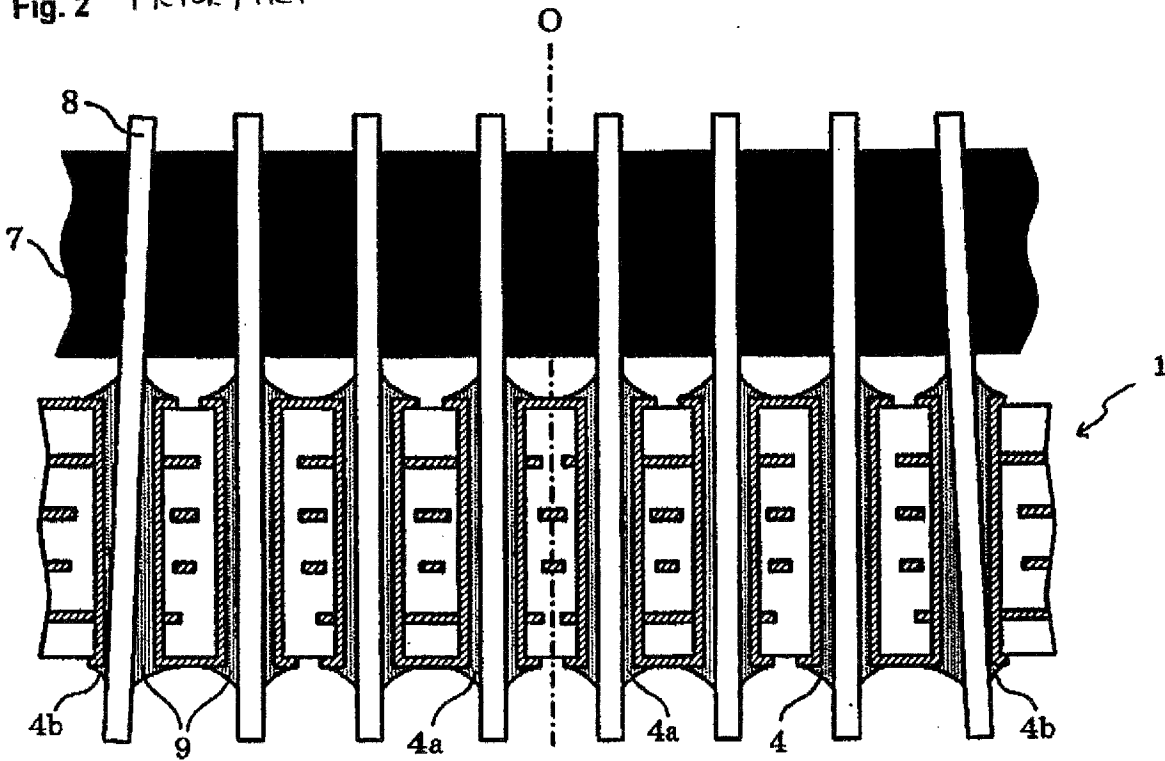
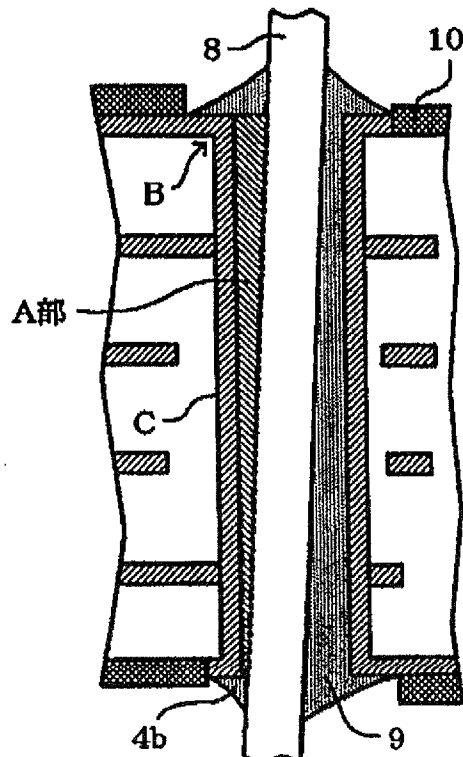


Fig. 3A PRIOR ART



**Fig. 3B** *Prior Art*

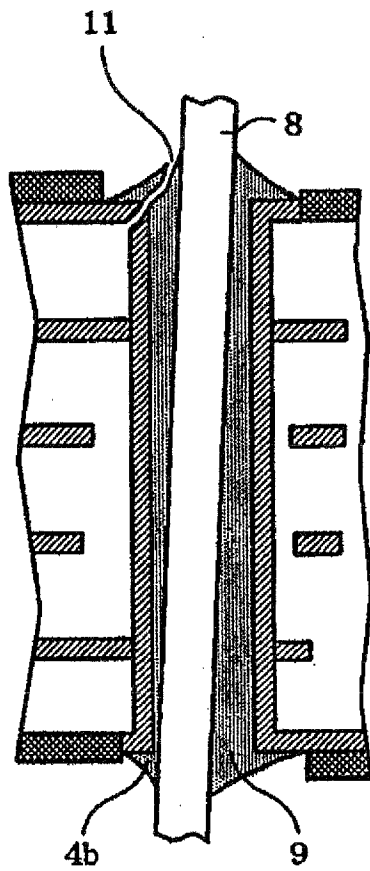




Fig. 3C *Prior Art*

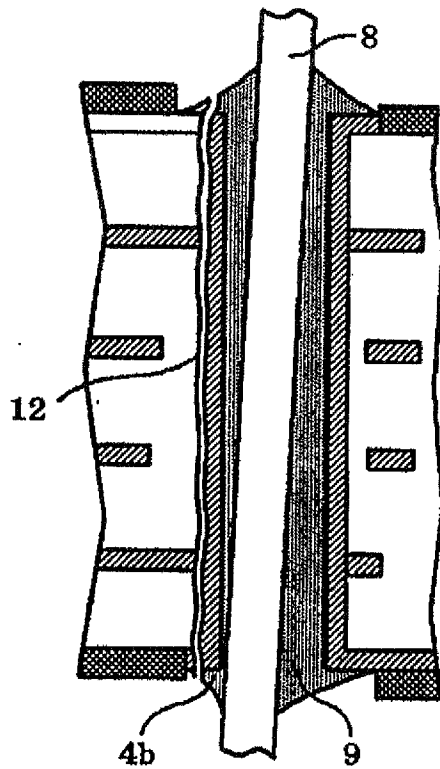
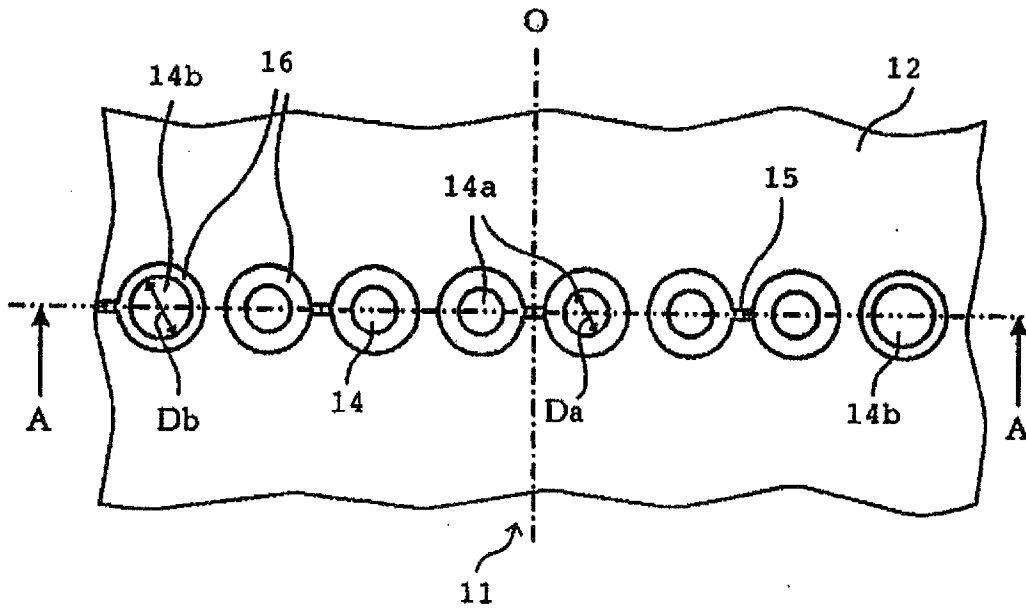


Fig. 4A



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Replacement Drawings